Chapter 7

HEAVY ION INDUCED EFFECTS IN VLSI DEVICES

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7.1 Introduction

The space environment of the Low Earth Orbit (LEO) and the Geostationary Earth Orbit (GEO) contain high-energy particulate radiation at energy levels of a few MeV to hundreds of MeV. As a result, the components used in various subsystems of the spacecraft get exposed to these particulate radiation. The high-energy particles impinging on VLSI devices can cause Single Event Effects (SEE) resulting in malfunction, device degradation or total failure of the device. Spacecraft system, in the recent years, use radiation hardened hi-reliability integrated circuits (ICs). Radhard IC's have protection against both Total Ionizing Dose (TID) effects and SEE induced by high-energy heavy ions. However, several Very Large Scale Integrated (VLSI) devices which are not available in radiation hardened versions are still required to used in specific space applications.

Spacecraft subsystems use different VLSI devices such as microprocessors, peripherals for microprocessors, application specific integrated circuits (ASIC), field programmable gate array (FPGA), high-density memories, MIL-STD-1553 Bus devices etc., in addition to other active devices. ASIC and FPGA and their subsystems are interfaced with MIL-STD-1553 bus interface configuration which uses 1553 bus controller/remote terminal integrated circuits. Some of these devices are available in radiation-hardened version and are tested at source by the manufacturer/Defence Supply Centre, Colombia / Jet Propulsion Lab (JPL) and other space customers. There are a few device types, which are not available in radiation hardened version but are required to be used in the spacecraft system. Such components need to be subjected to heavy ion irradiation and tested for their tolerance and suitability in space application. SEEs become more significant as the feature dimension/geometry of device decreases. VLSI devices made by sub-micron technology are particularly known to be very sensitive to high-energy particulate radiation. It is therefore important to carry out radiation testing and characterization of VLSI devices for heavy ion induced effects. Devices with feature dimension less than 5 ìm need to be characterised for SEE effects. American Society for Testing and Materials (ASTM) test method F1192M95 describes the methodology to carry out SEE characterization.

This chapter describes the results of heavy ion testing of few QML Class V, class H-grade VLSI devices for SEE. Heavy ion testing for SEE has been carried out on the following types of devices using five types of ions namely Si, Cl, Ti, Ni, and Ag:

- Field Programmable Gate Array (FPGA) RT 1280 (Rad Tolerant Version) of M/s. Actel, USA.
- 1553 Bus Controller, BU 61580 (Class H-grade) of M/s. ILC-DDC, USA.
- 1553 Bus Controller, Summit, 69151 DXE (Class V) of M/s. Aeroflex-UTMC, USA.

A low flux irradiation set-up available at Nuclear Science Centre (NSC), New Delhi, has been utilized for this purpose. This set-up can provide heavy ion beams with LET in the range of 1-70 MeV-cm^2/mg.

In the following sections a brief description of the different heavy ion induced SEEs, their mechanism and method of estimation of SEU rates are given.

7.2 Single Event Effects

SEE refers to the ionizing effect due to a single high-energy particle as it strikes the sensitive nodes (or sensitive volume) within the electronic device. Single event phenomenon can be classify into three effects

(a) Single Event Upset (SEU)

(b) Single Event Latchup (SEL)

(c) Single Event Burnout (SEB)

7.2.1 Single Event Upset

Single event upset is defined by NASA as "radiation-induced errors in microelectronic circuits caused when charged particles (usually from the radiation belts or from cosmic rays) lose energy by ionizing the medium through which they pass, leaving behind a wake of electron-hole pairs." SEU are transient soft errors and are non-destructive. A reset or rewriting of the device results in normal device behavior thereafter. An SEU may occur in analog, digital or optical components, or may have effects in surrounding interface circuitry. SEUs typically appear as transient pulses in logic or support circuitry, or as bit flips in memory cells or registers. Also possible is a multiple-bit SEU in which a single ion hits two or more bits causing simultaneous errors. Multiple-bit SEU is a problem for single-bit *error detection and correction* (EDAC) where it is impossible to assign bits within a word to different chips (for example, a problem for Dynamic Random

Access Memory (DRAM) and certain Static Random Access Memory (SRAM)). A severe SEU is the single-event functional interrupt (SEFI) in which an SEU in the device's control circuitry places the device into a test mode, halt or undefined state. The SEFI halts normal operations and requires reset to recover.

7.2.2 Single Event Latchup

Single event latchup is a condition that causes loss of device functionality due to a single event induced current state. Kolasinski et al. first observed SEL in 1979 during ground testing [1]. SELs are hard errors and are potentially destructive (i.e., they may cause permanent damage). The SEL results in high operating current, above device specifications. The latched condition can destroy the device, drag down the bus voltage, or damage the power supply. Originally, the concern was latchup caused by heavy ions. However, latchup can be caused by proton in very sensitive devices [2,3]. An SEL can be cleared by a power OFF-ON reset or power strobing of the device. If power is not removed quickly, catastrophic failure may occur due to excessive heating or metallization or bond wire failure. SEL is strongly temperature dependent: the threshold for latchup decreases at high temperature and the cross section increases as well [4,5].

7.2.3 Single Event Burnout

Single event burnout is a condition that can cause device destruction due to a high current state in a power transistor. SEB causes the device to fail permanently. SEBs include burnout of power Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), gate rupture, frozen bits and noise in CCDs (charge-copled devices). SEB of power MOSFETs was first reported by Waskiewicz et al [6]. Only SEB of n-channel power MOSFETs has been reported. An SEB can be triggered in a power MOSFET biased in the OFF state (i.e. blocking a high drain-source voltage) when a heavy ion passing through deposits enough charge to turn the device ON. SEB susceptibility has been shown to decrease with increasing temperature [7,8].

A power MOSFET may undergo *single-event gate rupture* (SEGR), which is the formation of a conducting path (i.e. localized dielectric breakdown) in the gate oxide resulting in a destructive burnout. The first report on SEGR of power MOSFETs was by Fischer in 1987 [9]. SEB can also occur in bipolar junction transistors as was first reported by Titus et al [10]. Swift et al. have described a new hard error, called *single-event dielectric rupture* (SEDR). SEDR (also referred to as micro-damage) occurs in Complimentary Metal Oxide Semiconductor (CMOS) devices and is similar to SEGR observed in power MOSFETs [11].

7.3. SEU mechanism and sensitivity

SEU can occur either because of direct ionization by heavy ion or by the products of nuclear reactions initiated by protons that occur in the device near the sensitive volume [12,13]. The sensitivity region in devices are the *p-n* junctions which have a voltage across them. In the CMOS flip-flop circuits shown in Figure 7.1, transistors N_1 and P_2 which are in the OFF state are sensitive. An ion passing through the *p-n* junction of N_1 produces electron-hole pairs along its path. These charges get separated in the *n-p* junction field and hence the node A gets negatively charged. This results in a negative spike at the node A. If the amplitude of voltage spike is sufficiently large, it turns ON the transistor P_2, and turns OFF the transistor N_2. Similarly if the ion passes through the transistor P_2 which is also in the OFF state, holes will be collected at the node B. If this voltage spike is sufficiently large, it will turn ON the transistor N_1 and turn OFF the transistor P_1.

For the bit error to occur, the voltage spike due to ionization charges (generated in the fraction of a nano-second) must be sufficiently large and hence a minimum amount of charge known as critical charge Q_c must be collected at the sensitive node. Critical charge Q_c depends upon the feature size of the device [13,14].

In addition to charges produced in the space charge region of the *p-n* junction, charges produced away from the junction along a portion of the ion path also contributes to SEU. This is known as funnel effect [15]. Upset rates can be diminished in two ways: by reducing the charge collection capability of the sensitive node as is employed in Silicon On Suphire (SOS), Silicon On Insulation (SOI) and Epi device manufacturing technology, and also by designing the bit cell so that it requires greater critical charge. By increasing the RC time constant of the gate capacitance, critical charge required to produce upset can be increased. For example in Figure 7.1, the resistance Rg reduces the height of the voltage spike appearing at the transistor P_2 [16]. The SEU susceptibility of different device manufacturing technologies is shown in Table 7.1.

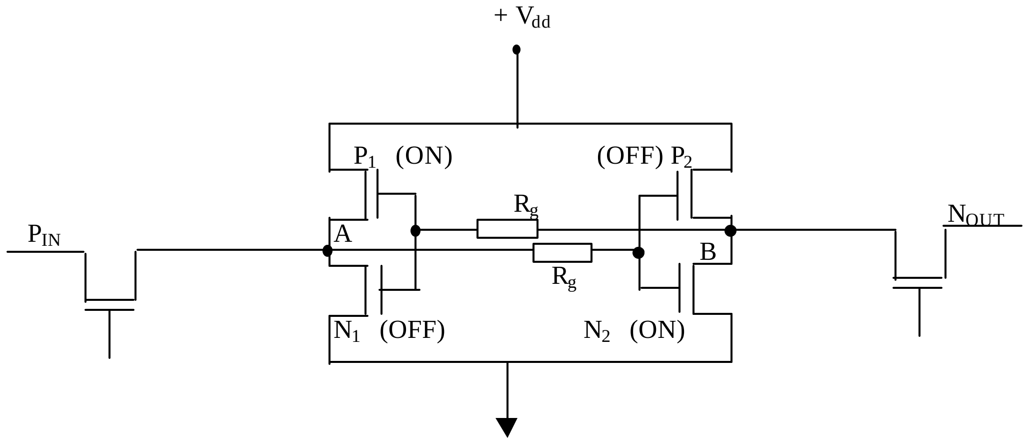

Figure 7.1 CMOS Flip-Flop.

Table. 7.1 SEU susceptibility of different device manufacturing technologies.

SEU Suceptibility of Device manufacturing Technologies	
CMOS / SOS	Least susceptible
CMOS	Intermediate susceptible
Standard bipolar	Intermediate susceptible
Low power Schottky bipolar	Intermediate susceptible
NMOS DRAMs	Most susceptible

SEU sensitivity of CMOS SRAMs increases with the total dose. Upto 200 krads, increase in SEU sensitivity is small and above 500 krads it is very significant [17]. But in the case of MOS DRAMs, SEU rate decreases with the increase of total dose [18].

7.4 SEU rate estimation method

SEU rate depends upon the SEU sensitivity of the devices and the particle flux in the environment. Space environment is described by Linear Energy Transfer (LET or dE/dX) spectrum which consists of flux of ions from atomic number 1 to 92. Device sensitivity is characterized by two parameters viz. upset cross-section (cm^2) and LET threshold L_{th} (MeV-cm^2/mg) which are measured by experiments. Upset cross-section is the ratio of number of upsets observed to the total flux (#/cm^2) of ions. Charge production by an ion depends upon the ion type, its energy and the device material. Charge produced is proportional to the LET of the ion, defined as dE/dX (MeV/µm or pC/µm or MeV-cm^2/mg).

LET of protons are small compared to heavy ions and thus can not deposit charge greater than Q_c by direct ionization in devices whose feature sizes are greater than one micron. But protons can initiate several kinds of nuclear reactions with Si, P, B and produce ions like He, O, N, C, Na and recoil Si. Most of the fragments of nuclear reactions have LETs around or less than 10 MeV-cm^2/mg and can deposit charges greater than Q_c of the devices. On the other hand, LETs of heavy ions are sufficiently large enough to deposit charge greater than the critical charge Q_c by ionization so that the voltage spikes at the sensitive nodes are large. Since the mechanism of SEUs by heavy ions and protons differ, the methods of SEU rate estimations are also quite different. However, testing of VLSI devices with heavy ion gives better information than with proton.

7.4.1 Estimation of SEU rate due to direct ionization

For calculating error rate E_R due to direct ionization by particles coming from outside the spacecraft, a parallelopiped sensitive volume is assumed with dimensions l, w and h (micron). The amount of charge deposited in this sensitive volume depends upon the path length (S) and the LET (L) of the particle since $Q = LS$. If D(S) is the probability that an ion will have a path length S in a parallelopiped, then all ions with path length S and $L \geq Q_c/S$ should produce upset. In other words all ions having LET L and path length $S \geq Q_c/L$ should produce upset. The error rate is then given by the equation [19].

$$E_R = \int_{S_{min}}^{S_{max}} \Phi(L)\; D(S)\, dS \tag{7.1}$$

where A is the average projected area of parallelopiped on the normal to the ion direction, Φ(L) is the omnidirectional integral LET flux, D[S(L)] is the probability that an ion will have a path length S in the parallelopiped sensitive volume for omnidirectional flux.

$$S_{\max} = \sqrt{l^2 + w^2 + h^2}$$

where *l, w, h* are in µm

$$S_{\min} = \frac{Q_c}{L_{\max}}$$

Q_C is expressed in pC, L in pC/μm, S in μm

$S \geq \frac{Q_c}{L}$ therefore, $dS = -\frac{Q_c}{L^2} dL$

Changing integral limits from S to L in equation (7.1), the error rate is given by

$$E_R = A \int_{L_{\max}}^{L_{\min}} -\frac{Q_c}{L^2} \Phi(L)\, D[S(L)]\, dL \tag{7.2}$$

$$E_R = Q_c\, A \int_{L_{\min}}^{L_{\max}} \Phi(L)\, D[S(L)] \frac{dL}{L^2} \tag{7.3}$$

Converting Q_c in pC to MeV and S_{max} in μm to gm/cm^2, L changes to MeV-cm^2 /g. Then equation (7.1) can be expressed as

$$E_R = 22.5\; Q_c\, A \int_{L_{\min}}^{L_{\max}} \Phi(L)\, D[S(L)] \frac{dL}{L^2} \tag{7.4}$$

where $L_{\min} = \frac{22.5 Q_c}{S_{\max}}$

is the minimum LET (MeV-cm^2/g) of an ion which can produce upset. It corresponds to the maximum path length S_{max} of an ion in the parallelopiped.

$$S_{\max} = 2.33 \times 10^{-4} \sqrt{l^2 + w^2 + h^2} \quad \text{g/cm}^2$$

A = (½) (*lw* + *wh* +*hl*) is the average projected area of the parallelopiped. The constant 22.5 converts pico-coulombs into MeV assuming 3.6 eV per electron-hole pair. Equation (7.4) has been used in the software *SE Analyst* to calculate SEU error rate due to direct ionization [20]. Input parameters for *SE Analyst* are the critical charge Q_c (pC) and the dimension l, w, h (μm) of the parallelopiped representing the sensitive volume of the device. These parameters should be determined by conducting heavy ion tests. SEU cross-section is the rate of number of upsets observed to the total flux (#/cm^2).

$$\text{Device cross-section (cm}^2) = \frac{\text{Number of upsets}}{\text{Total number of ions per cm}^2} \tag{7.5}$$

Source of heavy ions with LET values ranging from 1 to 45 MeV-cm^2/mg are required to determine saturation value of cross-section and the LET threshold value. Energy of ions should be chosen such that they penetrate at least 20 μm into the devices. LETs of all nucleons from Z = 1 to 92 at different energies are available from Transport of Ions in Matter (TRIM) calculations [21,22]. Measured heavy ion cross-section can vary from 10^{-5} to 10^{-10} upsets/bit/cm^2.

7.5 Experimental setup

Typically an ion current of 0.1 pna (particle nano amperes) is obtained from the particle accelerator. If the beam is spread over an area of 1 cm^2, it corresponds to flux of about 6×10^8 ions/cm^2/s. Therefore the direct ion beam irradiation gives a flux of the order of about 10^8 ions/cm^2/s or higher. In order to study SEE, low flux beam is required. Low flux beam require low beam currents, which cannot be controlled by settings of the pelletron machine. For low flux irradiation, one needs to adopt the technique of reducing the direct beam of ion fluxes. In the present work, we have used an add-on setup in the General Purpose Scattering Chamber (GPSC) beam line of the pelletron facility at the

NSC, New Delhi. The schematic diagram of the low flux irradiation set up installed at 20^0 port of the GPSC is shown in Figure 7.2. This set-up enables irradiation of the devices at low flux $<10^3$ ions/cm^2/s which is adequate for studying SEE. The set-up utilizes the scattering of direct beams from a gold foil of thickness ~330 nm. The high energy direct ion beam is made incident on the target foil kept at the center of GPSC. The flux of the outgoing ions after scattering is dependent on the thickness of the scatterer and the incoming ion flux and can be estimated using the surface barrier detector. The scattered ions are made to incident on the devices mounted on the target ladder. Normally, heavy ion tests are carried out on decapped devices (the die being directly exposed to ions at 90^0 incidence) since these particles cannot penetrate the device lid which is normally 1-3 mm thick KOVAR material. The decapped devices are irradiated in the active mode and the connections are taken out through hermetically sealed connectors for monitoring the ion-induced effects. Functional test patterns are generated for on-line monitoring during irradiation so that they bring out the effect of ion-induced faults [23]. Both SEU and SEL are monitored during tests. Though upsets can occur due to heavy ions with LET greater than 40 MeV-cm^2/mg, the probability is very small because of very low flux [24].

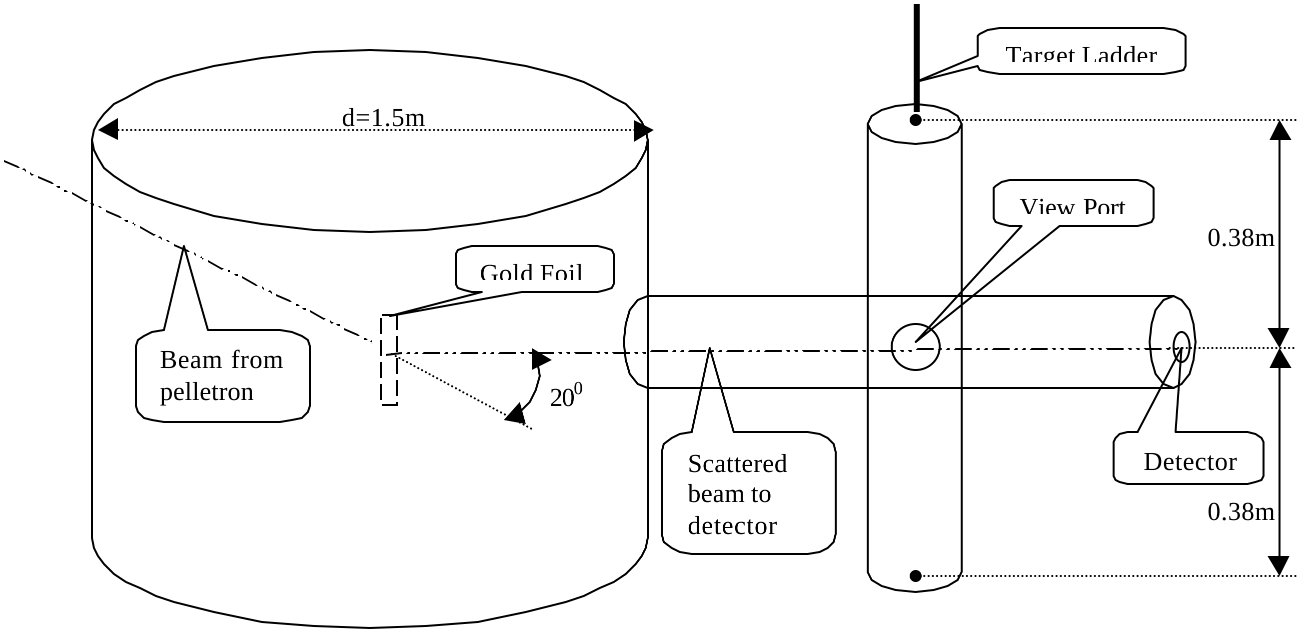

Figure 7.2 General Purpose Scattering Chamber with add-on set-up for SEE studies with heavy ions.

7.6 Results and discussion

The type of the devices investigated, the ions used for irradiation, LET, the flux of the ions and the summary of the results are tabulated in Table 7.2 and Table 7.3. The LET for different ions were calculated using the TRIM programme.

7.6.1 FPGA RT1280

FPGA RT1280 has 624 sequential and 608 combination modules. The sequential modules are storage modules. Hence, these are susceptible for SEU. To check all these sequential modules, a test circuit has been made inside FPGA creating 8 blocks (y1 to y8) of D-latches. Each block consists of an array of 8 x 8 D-latches. In a given block, ‘0’s and ‘1’s are stored alternatively in each row and column. The data pattern stored in each block is complimentary to that in the previous block. The monitoring circuit mounted outside the GPSC consists of 8 LEDs each representing a particular block. If an SEU occurs in any one D-latch of a block, it is indicated by the OFF state of the LED. Test set-up for FPGA is shown in the Figure 7.3. However, this test set-up does not indicate the number of SEUs occurring in each block.

Exposure of FPGA to Si^{8+} and Ti^{10+} ion beam has resulted in no SEL or SEU. However, when exposed to Ni ion beam, although no SEL has been observed even upto an LET of 32 MeV-cm^2/mg, SEUs have been observed in y2, y5, y6 and y7 blocks. Thus the LET threshold for SEL in this device is greater than 32 MeV-cm^2/mg. Additional tests at higher LET would be required to determine the SEL sensitivity of the device. The LET threshold for SEU is between 23 and 32 MeV-cm^2/mg. Since these LET thresholds are

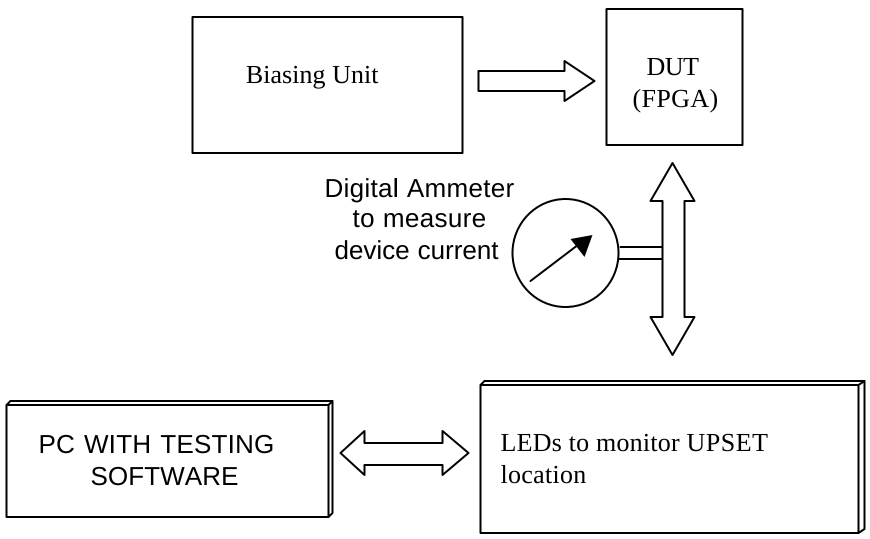

Figure 7.3 Test set-up for FPGA RT1280.

Table 7.2 FPGA RT 1280 test results.

Ion	Energy (MeV)	LET (MeV-cm^2/mg)	Flux (ions/cm^2/s)	Fluence (ions/cm^2)	Results	
					SEU	SEL
$^{28}Si^{8+}$	100	11	370	10^6	No upset	No latchup
$^{48}Ti^{10+}$	120	23	325	10^6	No upset	No latchup
$^{59}Ni^{10+}$	120	32	1000	10^6	SEU in y2 and y5 blocks	No latchup
$^{59}Ni^{10+}$	120	32	1000	10^6	SEU in y6 and y7 blocks	No latchup

greater than 15 MeV-cm^2/mg, it appears that proton irradiation is unlikely to produce SEU errors.

If the device dimension and sensitive nodes present in the devices are known, then upset rate can be calculated by using the equation (7.4). For FPGA the device parameters are not available. Hence, it is not possible to calculate the upset rates. Device cross-section can be calculated using the relation (7.5). Exposure of device to Si^{8+} (100 MeV) and Ti^{10+} (120 MeV) has not resulted in any upsets. However, irradiation by Ni^{10+} (120 MeV) ions results in few upsets. An estimation using equation 7.5 shows that the device cross-section for Ni is found to be 10^{-5} cm^2 (that is, for every 10^5 ions hitting the device one upset is observed).

7.6.2 Bus Controller

MIL-STD 1553 Bus Controller/Remote Terminal chip

A functional test circuit was made to operate the device in both Bus Controller (BC) mode and Remote Terminal (RT) mode alternatively as shown in Figure 7.4. In both the modes, the data transmission and reception were performed continuously [25-27]. The device has two bi-directional buses: Bus A and Bus B for transmission/reception of data operating continuously. The following tests were performed during irradiation:

- When the device is configured as bus controller, during ion irradiation it is checked for (a) proper transmission of data on both Bus A and Bus B, (b) proper reception of data on both Bus A and Bus B and (c) upsets in configuration register and in internal memory (in the case of ILC-DDC device).

- When the device is configured as Remote Terminal, it is checked for (a) proper transmission of data on both Bus A and Bus B (b) proper reception of data on both Bus A and Bus B.

Heavy ion testing of this devices has resulted in following results:

(i) 1553 Bus Controller summit IC from Aeroflex-UTMC, when subjected to Ag ion irradiation has resulted in two types of errors:

    (a) Upsets in configuration registers,
    (b) Errors in data transfer.

(ii) BU 61580 from ILC-DDC, USA testing has resulted in a number of upsets and functional failures for Cl ions. Its LET threshold for SEU is less than 11 MeV-cm^2/mg and for SEL is less than 15 MeV-cm^2/mg.

Information about the device dimension and sensitive nodes present in the device is not available. Hence, the upset rate could not be calculated. But device cross-section has been calculated using the relation (7.5). In the case of 1553 Bus Controller BU61580 VI-602, approximately 5000 upsets were experimentally observed when exposed to Si^{9+} (110 MeV) and Cl^{9+} (110 MeV). The device cross-section is then found to be 5 x 10^{-3} cm^2. In the case of 1553 Bus Controller Summit UT69151 DXE, only two upsets for 65 MeV Ag^{8+} ions were observed. The device cross-section is found to be 2 x 10^{-6} cm^2.

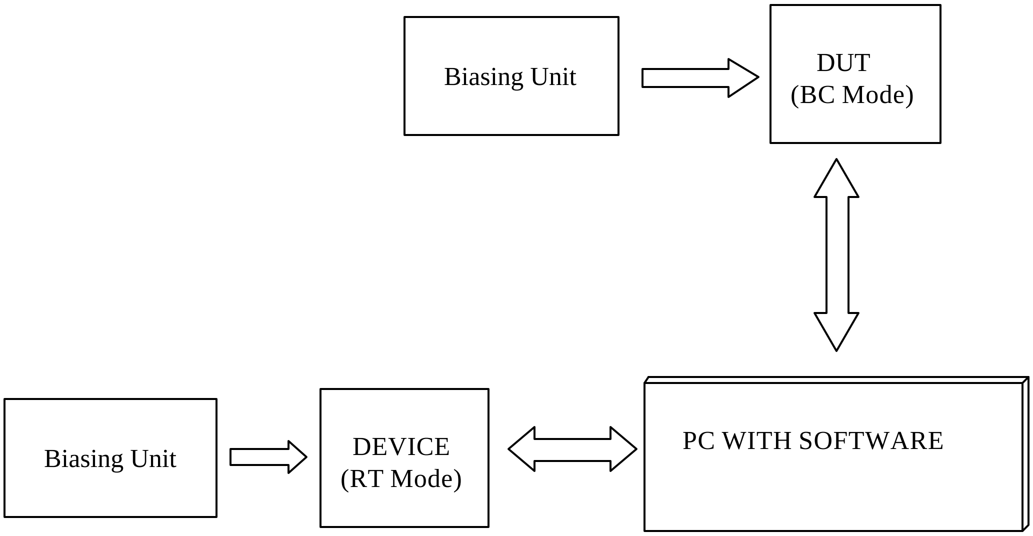

Figure 7.4 Test set-up for 1553 Bus Controller.

Table 7.3 Bus Controller test results.

Device	Ion	Energy (MeV)	LET (MeV-cm^2/mg)	Flux (ions/cm^2/s)	Fluence (ions/cm^2)	Results	
						SEU	SEL
1553 Bus Controller BU61580-V1-602	$^{48}Ti^{10+}$	120	23	400	3 x 10^3	Upsets not monitored	Latchup observed. Supply current increased from 65mA to 1.9 A
	$^{28}Si^{9+}$	110	11	370	10^6	Large number of upsets & functional failure	No latchup
	$^{36}Cl^{9+}$	110	15	225	10^6	Large number of upset & functional failure	Latchup observed
1553 Bus Controller Summit UT69151 DXE	$^{48}Ti^{10+}$	120	22	325	10^6	No upsets	No latchup
	$^{107}Ag^{8+}$	65	40	9500	10^6	2 upsets	No latchup

Based on the results obtained for heavy ions testing of the investigated devices, the following inference may be drawn:

- FPGA does not appear to be susceptible to SEL even though a few upsets are observed. The device may be used for LEO applications.
- Summit 69151 DXE MIL-STD-1553 Bus Controller appears to have high SEU LET and latch up immunity and thus appears to be suitable for space applications.
- BU 61580 MIL-STD-1553 Bus Controller appears to be vulnerable to SEE and hence may not be suitable for space applications.

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